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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,310	09/11/2003	Richard L. Coulson	ITL.1029US (P16765)	5388

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EXAMINER	
BHAT, ADITYA S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,310	COULSON ET AL.	
	Examiner	Art Unit	
	Aditya S. Bhat	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7,9,13-16,26-28 and 33-45* is/are rejected.

7)☒ Claim(s) *4-6,8,10-12,17-25 and 29-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 13, 26, and 35 are objected to because of the following informalities: The above mentioned claims recite the limitation "the temperature" in lines 2, 4, 5 and 2 respectively. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2 .The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 43 is rejected under 35 U.S.C. 102(e) as being anticipated by Gudesen et al. (WO 2004/025658)

With regards to claim 43, Watanabe (USPN 5,598,395) teaches an integrated circuit comprising: a ferroelectric polymer memory array; and a temperature sensor. (Page 9, lines 29-30)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gudesen et al. (WO 2004/025658) in view of Neufeld (USPN 5,974,438).

With regards to claim 44-45, Watanabe (USPN 5,598,395) does not explicitly teach the array is a cache memory is a disc cache memory.

Neufeld (USPN 5,974,438) teaches the memory array is a disc cache memory.(104c,106c, 107c,134;figure 1)

It would have been obvious to one skilled in the art at the time of the invention to modify Gudesen et al. (WO 2004/025658) to include a disc cache memory taught by Neufeld (USPN 5,974,438) in order minimize delays incurred when cache miss is encountered (Col. 3-4, lines 67 &1)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims1-3, 7, 9, 13-16, 21, 26-28 and 33-42 rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (USPN 5,598,395) in view of Neufeld (USPN 5,974,438).

With regards to claims 1 and 13, Watanabe (USPN 5,598,395)) teaches a method comprising, or an article comprising a medium storing instructions that, if executed, enable a processor based system to

monitoring a temperature; (S1;figure 3) and

in response to a detection of a temperature condition (S4;figure 3), transitioning the cache memory from a write-back cache to a write-through cache. (S8A;figure 3)

With regards to claim 3, Watanabe (USPN 5,598,395)) teaches adjusting the operation of a system using said memory at a first temperature and, in response to the detection of a higher, second temperature, transitioning the cache from a write-back cache to a write-through cache. (Col.6, lines 1-8).

With regards to claim 7 and 16, Watanabe (USPN 5,598,395) teaches shutting off the said cache memory at a temperature above said second temperature. (Col.6, lines 1-8).

With regards to claim 9, Watanabe (USPN 5,598,395) teaches upon detecting a lower temperature, resuming operation of said cache memory. (Figure 3)

With regards to claim 15, Watanabe (USPN 5,598,395) teaches storing instructions that, if executed, enable a processor-based system to adjust the operation of a system using said memory at a first temperature and, in response to the detection of a higher, second temperature, transition the cache memory from a write-back to a write-through cache. (Col.5, lines 11-65)

With regards to claim 21, Watanabe (USPN 5,598,395) teaches a processor based system to shut off the cache and invalidate all the cache lines. (s9;figure 3)

With regards to claim 26, Watanabe (USPN 5,598,395) teaches a processor-based system comprising:

a processor; (6;figure 1)

a disk drive coupled to said processor; (10, 20;figure 1)

a cache memory coupled said processor; (9;figure 1)and

a storage(8;figure 1) to store a cache driver to monitor a temperature and in response to the detection of a temperature condition, transition the cache memory from a write-back cache memory to a write-through cache memory(S8A;figure 3).

With regards to claim 33, Watanabe (USPN 5,598,395) teaches a storage, stores instructions that enable the system to resume cache operations after shutting off the cache memory in response to a cache condition by initially resuming reduced speed operations in a first stage and thereafter resuming normal operations. (8;figure 1)

With regards to claim 35, Watanabe (USPN 5,598,395) teaches a circuit comprising:

a component to receive an indication of a temperature and to develop a signal to transition the cache memory from a write-back cache to a write-through cache in response to said temperature indication. (6; figure 1)

With regards to claim 36, Watanabe (USPN 5,598,395) teaches a component to vary the operation of a system to adjust for the temperature affected operation of said cache memory. (figure 3)

With regards to claim 37, Watanabe (USPN 5,598,395) teaches a component to adjust a caching operation of the system in response to a temperature indication from said memory. (figure 3)

With regards to claim 38-39, Watanabe (USPN 5,598,395) teaches a component to shut off said cache in response to a temperature indication. (S9;figure 4)

With regards to claim 2, 14, 27-28, 34, and 40-42 Watanabe (USPN 5,598,395) does not appear to explicitly disclose monitoring the temperature of a ferroelectric polymer cache memory, a cache memory includes a temperature sensor.

Gudesen et al. (WO 2004/025658) discloses monitoring the temperature of a ferroelectric polymer cache memory, a cache memory includes a temperature sensor. (Page 9, lines 29-30)

It would have been obvious to one skilled in the art at the time of the invention to modify Watanabe (USPN 5,598,395) with Gudesen et al. (WO 2004/025658) to include a temperature sensor to monitor a ferroelectric polymer cache memory in order to determine at least one parameter indicative of a change in the memory cell. (Page 9, lines 9-10).

Allowable Subject Matter

5. The following is a statement of reasons for the indication of allowable subject matter: Claims 4-6, 8, 10-12, 17-20, 22-25 and 29-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claim 1-45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Neufeld et al. (USPN 5,974,438) teaches a scoreboard for cached multithread processes (Col.14, lines 39-42), Loper et al. (USPN 5,870,616) a system and method for reducing power consumption in an electronic circuit Gudesen et al. (USPUB 2005/0073869) teaches a method for operating a ferroelectric operating of or electret memory device and a device of this kind, and Peters et al. (USPN 6,470,289) teaches a independently controlling passive and active cooling in a computer system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aditya Bhat
May 13,2005

John Barlow
Supervisory Patent Examiner
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